STIC Search Report
EIC 2100

STIC Database Tracking Number: 142692

TO: Kuen S Lu **Location: RND 3B02** **Art Unit : 2167** **Tuesday, January 18, 2005** **Case Serial Number: 10/062992**	**From: Carol Wong** **Location: EIC 2100** **RND – 4A30** **Phone: 272-3513** **carol.wong@uspto.gov**

Search Notes

Dear Examiner Lu,

Attached are the search results (from commercial databases) for your case.

If you wish to order the complete text of any document, pls submit request(s) directly to the EIC2100 Reference Staff located in RND-4B28.

Pls call if you have any questions or suggestions for additional terminology, or a different approach to searching the case. Finally, pls complete the attached Search Results Feedback Form, as the EIC/STIC is continually soliciting examiners' opinion of the search service.

Thanks,
Carol

save for Advisory & after

STIC EIC 2100 Search Request Form

142693

Today's Date: 1/18/2005

What date would you like to use to limit the search?
Priority Date: 1/31/2002 Other:

Name Kuen S. Lu

AU 2167 Examiner # 79991

Room # RAN, 3B02 Phone 24114

Serial # 10/062992

Format for Search Results (Circle One):
(PAPER) DISK EMAIL

Where have you searched so far?
(USP) DWPI (EPO) (JPO) (ACM) IBM TDB Citeseer Sun
IEEE INSPEC SPI Other google, Oracle

Is this a "Fast & Focused" Search Request? (Circle One) (YES) NO
A "Fast & Focused" Search is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2100 and on the EIC2100 NPL Web Page at http://ptoweb/patents/stic/stic-tc2100.htm.
Please complete by 12:00 Am/pm 1/19/05

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

please attached page for details (claim 11)

① data storage structure stores sub networks based on a parameter derived from the output function of the subnetwork
② sub-network performs an output function
③ data access manager that identifies and retrieves sub-network from data storage structure

STIC Searcher [illegible] Phone 272-3513
Date picked up 1/18/05 Date Completed 1/18/05

SIRA Search and Information Resources Administration

File 347:JAPIO Nov 1976-2004/Aug(Updated 041203)
(c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2005/UD,UM &UP=200504
(c) 2005 Thomson Derwent

Set	Items	Description
S1	1850	SUBNET? OR SUB()(NET OR NETS OR NETWORK?)
S2	455067	NETWORK? OR NET OR NETS
S3	130	S1(3N)(PORTION? OR SECTION? OR PART OR PARTS OR DIVID? OR SUBSET? OR SEGMENT? OR SUBDIVID? OR SUBDIVISION? OR DIVISION? OR REGION?)
S4	61	S1(3N)(SECTOR? ? OR ZONE? ? OR PARTIAL OR BRANCH? OR PARTITION? OR SUB()SET? ? OR AREA? ?)
S5	7	S1(3N)(COMPONENT? OR SUBCOMPONENT?)
S6	3241324	OUTPUT? OR OUT()(PUT??? ? OR PUTT??? ?) OR RESULT?
S7	193587	S6(5N)(PARAMETER? OR VARIABLE? OR ATTRIBUTE OR ATTRIBUTES OR VALUE OR VALUES OR FACTOR? ? OR FEATURE OR FEATURES)
S8	6916	S6(2W)FUNCTION? ?
S9	7	S8 AND (S1 OR S3:S5)
S10	10	S7 AND (S1 OR S3:S5)
S11	15	S9:S10
S12	15	IDPAT (sorted in duplicate/non-duplicate order)
S13	15	IDPAT (primary/non-duplicate records only)

13/9/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015875369 **Image available**
WPI Acc No: 2004-033200/200403
XRPX Acc No: N04-026293
Data storage structure for combinational logic synthesizer, stores each sub - network in terms of graph and set of local functions, based on specific parameters derived from output function of sub - network
Patent Assignee: HETZEL A (HETZ-I); TEIG S (TEIG-I)
Inventor: HETZEL A; TEIG S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030217026	A1	20031120	US 200262992	A	20020131	200403	B

Priority Applications (No Type Date): US 200262992 A 20020131
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030217026	A1		48	G06F-007/00	

Abstract (Basic): US 20030217026 A1
NOVELTY - The data storage structure stores each **sub - network** in terms of a graph that represents the topology of set of integrated circuit element of each **sub - network** , and set of local functions for each node of the graph, based on specific **parameters** derived from **output function** of **sub - network** .
DETAILED DESCRIPTION - AN INDEPENDENT CLAIM is also included for **sub - network** record management system.
USE - Data storage structure for storing **sub - network** in combinational logic synthesizer for design of integrated circuit (IC).
ADVANTAGE - The data storage structure which efficiently stores **sub network** using specific **parameters** derived form **output function** of **sub network** is obtained.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of software architecture of logic synthesizer
network data storage (105)
global optimizer (110)
data generator (115)
timing engine (120)
designing unit (135)
pp; 48 DwgNo 1/26
Title Terms: DATA; STORAGE; STRUCTURE; COMBINATION; LOGIC; SYNTHESISER; STORAGE; SUB; NETWORK; TERM; GRAPH; SET; LOCAL; FUNCTION; BASED; SPECIFIC ; PARAMETER; DERIVATIVE; OUTPUT; FUNCTION; SUB; NETWORK
Derwent Class: T01; U11
International Patent Class (Main): G06F-007/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-J15A2; T01-N02A2; U11-G09

13/9/2 (Item 2 from file: 350)

015683552 **Image available**
WPI Acc No: 2003-745741/200370
XRPX Acc No: N03-597439
Technology mapping method for designing integrated circuit, involves replacing selected candidate sub - network **in design with replacement** sub - network
Patent Assignee: HETZEL A (HETZ-I); TEIG S (TEIG-I)
Inventor: HETZEL A; TEIG S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030159115	A1	20030821	US 200262993	A	20020131	200370	B

Priority Applications (No Type Date): US 200262993 A 20020131
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030159115	A1		48	G06F-017/50	

Abstract (Basic): US 20030159115 A1
NOVELTY - A parameter for identifying a replacement **sub - network** that is bound to a 0.13 micron or 0.1 micron technology, is generated based on a set of **output functions** performed by selected candidate **sub - network** in the received design. The selected candidate **sub - network** is replaced with the identified replacement **sub - network** .
USE - For designing integrated circuit (IC).
ADVANTAGE - Enables superior mapping of networks that are not bound to any target library, to a particular target library.
DESCRIPTION OF DRAWING(S) - The figure shows a flowchart explaining replacement **sub - network** determination process.
pp; 48 DwgNo 14/26
Title Terms: TECHNOLOGY; MAP; METHOD; DESIGN; INTEGRATE; CIRCUIT; REPLACE; SELECT; CANDIDATE; SUB; NETWORK; DESIGN; REPLACE; SUB; NETWORK
Derwent Class: T01; U11
International Patent Class (Main): G06F-017/50
File Segment: EPI
Manual Codes (EPI/S-X): T01-J15A2; U11-G

13/9/3 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX
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015683224 **Image available**
WPI Acc No: 2003-745413/200370
XRPX Acc No: N03-597126
Data storage structure, includes set of sub - networks **that are stored based on set of indices derived from** output **functions of** sub - networks
Patent Assignee: HETZEL A (HETZ-I); TEIG S (TEIG-I)
Inventor: HETZEL A; TEIG S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030154210	A1	20030814	US 200261474	A	20020131	200370	B

Priority Applications (No Type Date): US 200261474 A 20020131
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030154210	A1		48	G06F-007/00	

Abstract (Basic): US 20030154210 A1
NOVELTY - The structure includes a set of **sub - networks** , each **sub - network** is stored based on a set of numerical indices that are present in a relational database of the structure. The set of indices for each of the **sub - network** includes a primary index and a set of secondary indices. The indices are derived from a set of **output functions** of the **sub - networks** .
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a **sub - network** record management system.
USE - Used for storing **sub - networks** .
ADVANTAGE - The indexing scheme stores and identifies the pre-tabulated **sub - networks** . The indexing scheme allows efficient identification and storing of the multi-function **sub networks** .
DESCRIPTION OF DRAWING(S) - The drawing shows the software architecture of a logic synthesizer.
Logic synthesizer (100)
Data generator (115)
Global optimizer (110)
Circuit network design (135)
Power engine (140)
pp; 48 DwgNo 1/26
Title Terms: DATA; STORAGE; STRUCTURE; SET; SUB; NETWORK; STORAGE; BASED; SET; INDEX; DERIVATIVE; OUTPUT; FUNCTION; SUB; NETWORK
Derwent Class: T01
International Patent Class (Main): G06F-007/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-F05E; T01-F05G5; T01-N02A2

13/9/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

015649021 **Image available**
WPI Acc No: 2003-711204/200367
XRPX Acc No: N03-568763
Technology mapping performing method for integrated circuit design, involves replacing selected sub - network **with replacement** sub - network **which is identified based on** parameter **representing** output

function **of selected** sub - network
Patent Assignee: HETZEL A (HETZ-I); TEIG S (TEIG-I)
Inventor: HETZEL A; TEIG S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030154449	A1	20030814	US 200261719	A	20020131	200367	B

Priority Applications (No Type Date): US 200261719 A 20020131
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030154449	A1		48	G06F-017/50	

Abstract (Basic): US 20030154449 A1

NOVELTY - A candidate **sub - network** with graph structure different from tree structure or micro-leaf directed acyclic graph structure is selected from a received design. A **parameter** is generated based on **output function** of the **sub - network** . A replacement **sub - network** is identified from a storage based on the parameter and replaced with selected **sub - network**

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for technology mapping performing program.

USE - For performing technology mapping in integrated circuit design.

ADVANTAGE - Allows efficient storing and identification of multi-element and multi-function **sub - network** .

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart explaining the technology mapping performing process.

pp; 48 DwgNo 2/26

Title Terms: TECHNOLOGY; MAP; PERFORMANCE; METHOD; INTEGRATE; CIRCUIT; DESIGN; REPLACE; SELECT; SUB; NETWORK; REPLACE; SUB; NETWORK; IDENTIFY; BASED; PARAMETER; REPRESENT; OUTPUT; FUNCTION; SELECT; SUB; NETWORK
Derwent Class: T01; U11
International Patent Class (Main): G06F-017/50
File Segment: EPI
Manual Codes (EPI/S-X): T01-J15A2; T01-S03; U11-G01

13/9/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011462761 **Image available**
WPI Acc No: 1997-440668/199741
XRPX Acc No: N97-366575
Communications association memory e.g. CAM between sub - networks **- has output transmission address corresponding to received address which is established per line to first latch circuit group**
Patent Assignee: ZH KANKOKU DENSHI TSUSHIN KENKYUSHO (KANK-N); KOREA ELECTRONICS & TELECOM RES (KOEL-N); KOREA TELECOM (KOTE-N)
Inventor: JEON J A; KIM J G; PARK Y H
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9198879	A	19970731	JP 96344321	A	19961224	199741	B
KR 97049598	A	19970729	KR 9619877	A	19960604	199908	

Priority Applications (No Type Date): KR 9555892 A 19951223
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes

JP 9198879 A 9 G11C-015/04
KR 97049598 A G06F-012/08
Abstract (Basic): JP 9198879 A

The memory outputs the transmission address corresponding to the received address. The received address is established per line to the first latch circuit group. The transmission address is established per line to the second latch circuit group. The set **value output** from each latch circuit is compared with first latch circuit by comparison detector.

Similarly the second latch circuit is compared. The reception return selection part selects the transmission address and transmission return selection part (16) selects the receiving address.

ADVANTAGE - Overcomes constraint of access time and delay of access. Provides high speed address conversion freely.

Dwg.2/5

Title Terms: COMMUNICATE; ASSOCIATE; MEMORY; CAM; SUB; NETWORK; OUTPUT; TRANSMISSION; ADDRESS; CORRESPOND; RECEIVE; ADDRESS; ESTABLISH; PER; LINE ; FIRST; LATCH; CIRCUIT; GROUP
Index Terms/Additional Words: CONTENT; ADDRESSABLE; MEMORY
Derwent Class: U14
International Patent Class (Main): G06F-012/08; G11C-015/04
File Segment: EPI
Manual Codes (EPI/S-X): U14-A05

13/9/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009916123 **Image available**
WPI Acc No: 1994-183833/199422
XRPX Acc No: N94-145124

Programmable logic device with groups of AND gates - some of the AND logic function gate groups having different numbers of logic input sets

Patent Assignee: INFINITE TECHNOLOGY CORP (INFI-N); NIPPON PRECISION CIRCUITS INC (NIPR-N); NIPPON PRECISION CIRCUITS KK (NIPR-N)
Inventor: JENNINGS E W; LANDERS G H
Number of Countries: 019 Number of Patents: 010
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9411950	A1	19940526	WO 93US10787	A	19931108	199422	B
JP 6224741	A	19940812	JP 93278368	A	19931108	199437	
JP 6224742	A	19940812	JP 93278369	A	19931108	199437	
US 5394030	A	19950228	US 92972993	A	19921110	199514	
EP 669057	A1	19950830	WO 93US10787	A	19931108	199539	
			EP 94901341	A	19931108		
EP 669057	A4	19960117	EP 94901341	A		199633	
US 5596766	A	19970121	US 92974193	A	19921110	199710	
			US 95390818	A	19950216		
KR 287538	B	20010416	WO 93US10787	A	19931108	200219	
			KR 95701844	A	19950509		
JP 3313849	B2	20020812	JP 93278369	A	19931108	200259	
JP 3313848	B2	20020812	JP 93278368	A	19931108	200259	

Priority Applications (No Type Date): US 92974193 A 19921110; US 92972993 A 19921110; US 95390818 A 19950216
Cited Patents: US 4124899; US 4642487; US 4742252; US 4872137; US 5136188; No-Citns.
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9411950	A1	E	7	H03K-019/177	

Designated States (National): KR
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE

JP 6224741	A	34	H03K-019/173	
JP 6224742	A	21	H03K-019/173	
US 5394030	A	24	H03K-019/177	
EP 669057	A1 E	7	H03K-019/177	Based on patent WO 9411950
	Designated States (Regional): DE FR GB IE NL			
EP 669057	A4		H03K-019/177	
US 5596766	A	35	G06F-009/305	Cont of application US 92974193
KR 287538	B		H03K-019/177	Previous Publ. patent KR 95704859 Based on patent WO 9411950
JP 3313849	B2	20	H03K-019/173	Previous Publ. patent JP 6224742
JP 3313848	B2	30	H03K-019/173	Previous Publ. patent JP 6224741

Abstract (Basic): WO 9411950 A

Each AND logic function gate group (SGA12...SGA1) has individual **output** AND logic **function** gates programmable by respective programmable logic function generators (PLFG) of a set.

Each PLFG has sets of logic inputs. Each PLFG can generate any logic function gates of each set of logic inputs for use as inputs to an **output** AND logic **function** gates according to programmable control inputs. Some of the AND logic function gate groups have different numbers of logic input sets (A0B0...A11B11). Each set of PLFGs receive the same sets of logic inputs.

USE/ADVANTAGE - Greater versatility of application, operating speed and optimisation of AND gate utilisation. Facilitates implementation of user programmable complex functions.

Dwg.1/33

Abstract (Equivalent): US 5596766 A

A configurable logic network having a plurality of programmable logic devices (PLD) coupled to a **sub - network** that is operable to perform logic operations using, logic instructions and logic values originating externally of the PLDs, under control of output logic control signals derived from said PLDs;

each programmable logic device comprising an AND logic array having inputs for receiving signals and generating product term output signals, OR logic array having inputs for receiving signals and generating sum term output signals, at least one of said logic arrays being programmable, said logic arrays interconnected to apply output signals from one of said AND and OR logic arrays as input signals to the other one of said AND and OR logic arrays, said other one of the AND and OR logic arrays providing PLD output signals;

a plurality of logic combination circuits coupled to at least one of said PLDs to receive selected ones of said PLD output signals and to produce at least one output logic control signal from each logic combination circuit as determined by the PLD output signals received by that logic combination circuit;

said **sub - network** comprising a controllable logic function **sub - network** operable to perform logic operations; inputs separate from said PLDs for supplying logic instructions and logic values to said **sub - network** for use in performing said logic operations; and

control logic circuitry coupling at least some of said logic combination circuits to said **sub - network** to supply selected ones of said output logic control signals to said **sub - network** to control routing within said **sub - network** of said logic instructions and logic values, including logic instructions and logic values generated by said **sub - network** in performing said logic operations.

Dwg.18/32

Title Terms: PROGRAM; LOGIC; DEVICE; GROUP; GATE; LOGIC; FUNCTION; GATE;

GROUP; NUMBER; LOGIC; INPUT; SET
Derwent Class: U21
International Patent Class (Main): G06F-009/305; H03K-019/173; H03K-019/177
International Patent Class (Additional): H01L-025/00
File Segment: EPI
Manual Codes (EPI/S-X): U21-C01E

13/9/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009865843 **Image available**
WPI Acc No: 1994-145714/199418
XRPX Acc No: N94-114814
Feed forward segmented neural network used in e.g. OCR - has pyramidal stack of network layers each made up of several sub - networks **formed of several nodes**
Patent Assignee: EASTMAN KODAK CO (EAST)
Inventor: BRYANT S M; LOEWENTHAL K H
Number of Countries: 001 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 595033	A2	19940504	EP 93115497	A	19930925	199418	B
EP 595033	A3	19941109	EP 93115497	A	19930925	199535	
US 5586223	A	19961217	US 92967987	A	19921027	199705	
			US 95389550	A	19950215		

Priority Applications (No Type Date): US 92967987 A 19921027; US 95389550 A 19950215
Cited Patents: No-SR.Pub; 3.Jnl.Ref; EP 459276; US 5063521
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 595033	A2	E	10	G06F-015/80	
US 5586223	A		10	G06F-015/80	Cont of application US 92967987
EP 595033	A3			G06F-015/80	

Abstract (Basic): EP 595033 A

The neural network includes several network layers and several **sub - networks** . Each **sub - network** resides within one of the network layers. Some of the layers have multiple **sub - networks** . All layers have at least one **sub** - network . In layers with multiple **sub - networks** , all the **sub - networks** are **segmented** from each other. The layers are arranged in pyramidal fashion from an input network layer to an output network layer.

The number of **sub - networks** in layers decreases from input to output layers. Each **sub - network** in hardware has a memory device. Each memory comprises either a RAM device or a PROM device and has more inputs than outputs.

USE/ADVANTAGE - In e.g. optical character recognition, pattern recognition, machine learning, process control, voice recognition. High speed. Reduced size and complexity.

Dwg.1/5

Abstract (Equivalent): US 5586223 A

A method for emulating a feed forward, segmented neural network having a large number of inputs, said method comprising the steps of:

(a) modeling a segmented neural network having a large number of inputs as multiple network layers of **subnetworks** **segmented** such that each **subnetwork** within a network layer receives totally different inputs than all other **subnetworks** within said network

layer, a plurality of said multiple network layers each having an even number of **segmented subnetworks** , each **subnetwork** comprising a plurality of interconnected sublayers, each sublayer having a plurality of processing nodes, and each **subnetwork** being sized for realization as a single binary memory device;

(b) training the segmented neural network modeled in step (a) while requiring that input and **output values** of each network layer comprise binary signals;

(c) mapping all possible input and corresponding **output values** of each **subnetwork** of said trained **segmented** neural network;

(d) storing the mapped input and **output values** of each **subnetwork** in an associated binary memory device such that behavior of each **subnetwork** of the trained **segmented** neural network is emulated completely by the associated binary memory device; and

(e) electrically interconnecting associated binary memory devices in a circuit arrangement corresponding to connection of the **subnetworks** in the modeled **segmented** neural network.

Dwg.5/5

Title Terms: FEED; FORWARD; SEGMENT; NEURAL; NETWORK; OCR; PYRAMID; STACK; NETWORK; LAYER; MADE; UP; SUB; NETWORK; FORMING; NODE
Index Terms/Additional Words: PATTERN; RECOGNITION; MACHINE; LEARNING; PROCESS; CONTROL; VOICE; RECOGNITION
Derwent Class: T01; T04
International Patent Class (Main): G06F-015/80
File Segment: EPI
Manual Codes (EPI/S-X): T01-C08A; T01-J16C1; T04-D04

13/9/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009727896 **Image available**
WPI Acc No: 1994-007746/199401
XRPX Acc No: N94-006257

Residual activation neural network for plant control - uses neural network to predict future error from desired state and applies this to inverse network to derive current control changes

Patent Assignee: PAVILION TECHNOLOGIES INC (PAVI-N); FERGUSON R B (FERG-I); HARTMAN E J (HART-I); KEELER J D (KEEL-I); LIANO K (LIAN-I)
Inventor: FERGUSON R B; HARTMAN E J; KEELER J D; LIANO K
Number of Countries: 022 Number of Patents: 012
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9325943	A2	19931223	WO 93US5596	A	19930610	199401	B
AU 9344114	A	19940104	AU 9344114	A	19930610	199417	
US 5353207	A	19941004	US 92896755	A	19920610	199439	
WO 9325943	A3	19940303	WO 93US5596	A	19930610	199515	
EP 645025	A1	19950329	EP 93914464	A	19930610	199517	
			WO 93US5596	A	19930610		
US 5559690	A	19960924	US 92896755	A	19920610	199644	
			US 94307521	A	19940916		
JP 9506986	W	19970708	WO 93US5596	A	19930610	199737	
			JP 94501743	A	19930610		
EP 645025	B1	19981104	EP 93914464	A	19930610	199848	
			WO 93US5596	A	19930610		
DE 69321952	E	19981210	DE 621952	A	19930610	199904	
			EP 93914464	A	19930610		
			WO 93US5596	A	19930610		
US 5859773	A	19990112	US 92896755	A	19920610	199910	

				US 94307521	A	19940916		
				US 96717719	A	19960923		
US 6363289	B1	20020326		US 96717719	A	19960923	200226	N
				US 99228962	A	19990112		
US 20020087221	A1	20020704		US 99228962	A	19990112	200247	N
				US 200241157	A	20020108		

Priority Applications (No Type Date): US 92896755 A 19920610; US 94307521 A 19940916; US 96717719 A 19960923; US 99228962 A 19990112; US 200241157 A 20020108

Cited Patents: 4.Jnl.Ref; EP 463934; EP 531712; US 4912753; US 4928484; No-SR.Pub

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9325943	A2	E	49	G05B-013/02	
Designated States (National): AU CA JP KP KR					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
AU 9344114	A			G05B-013/02	Based on patent WO 9325943
US 5353207	A		18	G06F-015/00	
WO 9325943	A3			G05B-013/02	
EP 645025	A1	E	2	G05B-013/02	Based on patent WO 9325943
Designated States (Regional): DE ES FR GB IT NL SE					
US 5559690	A		17	G05B-013/02	Cont of application US 92896755 Cont of patent US 5353207
JP 9506986	W		48	G05B-013/02	Based on patent WO 9325943
EP 645025	B1	E		G05B-013/02	Based on patent WO 9325943
Designated States (Regional): DE ES FR GB IT NL SE					
DE 69321952	E			G05B-013/02	Based on patent EP 645025 Based on patent WO 9325943
US 5859773	A			G05B-013/02	Cont of application US 92896755 Cont of application US 94307521 Cont of patent US 5353207 Cont of patent US 5559690
US 6363289	B1			G05B-013/02	Cont of application US 96717719 Cont of patent US 5859773
US 20020087221	A1			G05B-013/02	Cont of application US 99228962

Abstract (Basic): WO 9325943 A

A plant control system includes a number of neural networks to derive desired control actions. The control network(74) receives plant state variable(s(t)) and produces an accurate model of the plant output. The network has input, hidden and output layers.

The model output(oP(t)) is compared with a desired output(oD(t)) to give an error(E). This is fed into the inverse plant model(76) and iteratively used to derive a set of plant controls(c(t+1)) to be applied to the plant. There are a number of neural networks where the first gives a base estimation and the other are applied successively to residuals to improve prediction.

ADVANTAGE - Improves accuracy of control and identifies external perturbations.

Dwg.1/15

Abstract (Equivalent): US 5559690 A

A network for predicting plant outputs of a plant and for receiving control variables that are used to control the plant and measurable state variables of the plant, with the measurable state variables having dependencies on the control variables and unmeasurable external influences, the control network for projecting out the dependencies of the measurable state variables on the control variables, comprising:

a residual activation neural network for generating an estimation of the unmeasurable external influences on the plant and having:

an input layer for receiving the control variables,
an **output** layer for **outputting** predicted state **variables** ,
a hidden layer for mapping said input layer to said output layer through a representation of the dependencies of the state variables on the control variables to generate said predicted state variables, which said representation is trained on the measurable state variables, and
a residual layer for determining as a residual the difference between said predicted state variables and the input state variables, said residual comprising an estimation of the unmeasurable external influences on the plant; and
a main neural network having:
an input layer for receiving as inputs the control variables and input signals parameterized by said residual,
an output layer for outputting a predicted plant output, and
a hidden layer for mapping said input layer to said output layer through a representation of the plant as a function of the control variables and said residual.
Dwg.1/15
US 5353207 A
A plant (72) is operable to receive control inputs c(t) and provide an output y(t). The plant (72) has associated therewith state variables s(t) that are not variable. A control network (74) is provided that accurately models the plant (72). The output of the control network (74) provides a predicted output which is combined with a desired output to generate an error. This error is back propagated through an inverse control network (76), which is the inverse of the control network (74) to generate a control error signal that is input to a distributed control system (73) to vary the control inputs to the plant (72) in order to change the output y(t) to meet the desired output.
The control network (74) is comprised of a first network NET 1 that is operable to store a representation of the dependency of the control variables on the state **variables** . The predicted **result** is subtracted from the actual state variable input and stored as a residual in a residual layer. The output of the residual layer is input to a hidden layer which also receives the control inputs to generate a predicted output in an output layer. During back propagation of error, the residual values in the residual layer are latched and only the control inputs allowed to vary.
ADVANTAGE - Improves performance and accuracy in neural networks by utilising residual activation in **subnetworks** .
Dwg.7a/15
Title Terms: RESIDUE; ACTIVATE; NEURAL; NETWORK; PLANT; CONTROL; NEURAL; NETWORK; PREDICT; FUTURE; ERROR; STATE; APPLY; INVERSE; NETWORK; DERIVATIVE; CURRENT; CONTROL; CHANGE
Derwent Class: T01; T06
International Patent Class (Main): G05B-013/02; G06F-015/00
International Patent Class (Additional): G05B-011/32; G05B-013/00; G05B-013/04; G06F-015/18; G06F-019/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-J07; T01-J16C1; T06-A05A; T06-D10

13/9/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009533990 **Image available**
WPI Acc No: 1993-227531/199328
XRPX Acc No: N93-174599
Rapidly converging projective neural network - converts input patterns to numerical form and calculates dimensional projected input vectors which

are stored for comparison with goals to determine errors

Patent Assignee: R & D ASSOC (RDAS-N)
Inventor: MANUKIAN N; WILENSKY G D
Number of Countries: 038 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9313487	A1	19930708	WO 92US8319	A	19920930	199328	B
AU 9228692	A	19930728	AU 9228692	A	19920930	199347	
US 5276771	A	19940104	US 91814357	A	19911227	199402	
EP 619901	A1	19941019	EP 92922053	A	19920930	199440	
			WO 92US8319	A	19920930		
JP 7502357	W	19950309	WO 92US8319	A	19920930	199518	
			JP 93511618	A	19920930		

Priority Applications (No Type Date): US 91814357 A 19911227
Cited Patents: US 4914563; US 5058034; US 5060278
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9313487	A1		87	G06F-015/18	
Designated States (National): AU BB BG BR CA CS FI HU JP KP KR LK MG MN MW NO PL RO RU SD					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL OA SE					
AU 9228692	A			G06F-015/18	Based on patent WO 9313487
US 5276771	A		36	G06F-015/16	
EP 619901	A1	E	2	G06F-015/18	Based on patent WO 9313487
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LI LU MC NL SE					
JP 7502357	W		25	G06F-015/18	Based on patent WO 9313487

Abstract (Basic): WO 9313487 A

The appts. comprises a processor/controller (20) connected via an internal or external data and/or address bus (22) to an input unit (24), a projection unit (26), a neural connection unit (28), a network **output** storage unit (30), a goal **value** unit (32), a comparison unit (34) and an output unit (36).

The input unit, which may be a computer, converts input patterns in numerical form, having N numerical values that form the N-dimensional input vectors which are stored in a memory. The processor calculates the N+1 dimensional projected input vectors and stores these elements. The system compares network **output values** with known goal vectors and an error function is minimized. The network is sub- **divided** into **sub - networks** which are individually trained and recombined.

ADVANTAGE - Provides neural network with shorter training time whilst maintaining ability to find optimum solution making more efficient use of network with fewer nodes and weights.

Dwg.15/17

Abstract (Equivalent): US 5276771 A

A data processing system and method for solving pattern classification problems and function-fitting problems includes a neural network in which N-dimensional input vectors are augmented with at least one element to form an N+j dimensional projected input vector, whose magnitude is then preferably normalised to lie on the surface of a hypersphere. Weight vectors of at least a lowest intermediate layer of network nodes are preferably also constrained to lie on the N+j-dimensional surface.

To train the network, the system compares network **output values** with known goal vectors, and an error function (which depends on all weights and threshold **values** of the intermediate and **output** nodes) is then minimized. In order to decrease the network's learning time

even further, the weight vectors for the intermediate nodes are initially preferably set equal to known prototypes for the various classes of input vectors. The network may be separated into **sub - networks** , which are then trained individually and later recombined. The network is able to use both hyperspheres and hyperplanes to form decision boundaries, and, indeed, can converge to the one even if it initially assumes the other.

USE - Eg speech and handwriting recognition, robotic control, function fitting.

Dwg.15/17

Title Terms: RAPID; CONVERGE; PROJECT; NEURAL; NETWORK; CONVERT; INPUT; PATTERN; NUMERIC; FORM; CALCULATE; DIMENSION; PROJECT; INPUT; VECTOR; STORAGE; COMPARE; GOAL; DETERMINE; ERROR

Derwent Class: T01

International Patent Class (Main): G06F-015/16; G06F-015/18

File Segment: EPI

Manual Codes (EPI/S-X): T01-J04A; T01-J04C; T01-J16C1

13/9/12 (Item 12 from file: 350)

DIALOG(R)File 350:Derwent WPIX

008462774 **Image available**

WPI Acc No: 1990-349774/199047

XRPX Acc No: N90-267197

Deriving gradients from adaptive digital signal network - summing input signals and delaying signals with multiplication by internal signals

Patent Assignee: SIEMENS AG (SIEI)

Inventor: KUMMERT A

Number of Countries: 015 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 397912	A	19901122	EP 89109086	A	19890519	199047	B
JP 3006115	A	19910111	JP 90124334	A	19900516	199108	
US 5111418	A	19920505	US 90525163	A	19900517	199221	
EP 397912	B1	19940810	EP 89109086	A	19890519	199431	
DE 58908193	G	19940915	DE 508193	A	19890519	199436	
			EP 89109086	A	19890519		

Priority Applications (No Type Date): EP 89109086 A 19890519

Cited Patents: 3.Jnl.Ref

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 397912	A				
Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE					
US 5111418	A		13		
EP 397912	B1	G	20	H03H-021/00	
Designated States (Regional): DE FR GB IT NL					
DE 58908193	G			H03H-021/00	Based on patent EP 397912

Abstract (Basic): EP 397912 A

The adaptive digital filter network (NW) for processing discrete signals has a first stage (N1) receiving the input signals (X bar) and providing the filtered output signals (y bar) and a second stage (N2) delaying the signals (d bar) received from the first stage and feeding them back to the latter.$ Further output signals representing the gradient of the output signals relative to the filter network parameter (alpha bar) are obtained using all input signals (x bar), all delayed signals (c bar) provided by the second filter stage (N2) and all filter network parameters, together with internal recursive signals which have

the same delay as that provided by the second filter setage.$ ADVANTAGE - Simple provision of filter network output signal gradient. (16pp Dwg.No.2/7)

Abstract (Equivalent): EP 397912 B

Method for obtaining the gradient of output signals (y) of a network (NW) for processing discrete-time signals with respect to the network parameters (a), the network (NW) comprising a delay-free first **sub - network** (N1) which receives input signals (x) and which outputs the output signals (y), and a second **sub - network** (N2) having only delaying elements to which signals (d) from the first **sub - network** (N1), characterised in that further output signals corresponding to the gradient of the output signals (y) with respect to the network parameters (a) are formed in each case which are equal to the sum of all the signals produced by gating all the input signals (x), all the signals (c) delayed by the second **sub - network** (N2) and all the network parameters (a) by means of a first gating function, and of all the signals produced by gating all the input signals (x), all the signals (c) delayed by the second **sub - network** (N2) and all the network parameters (a) by means of a second gating function multiplied by internal signals that are delayed in accordance with the second **sub - network** (N2), in that the first gating function is equal to the gradient of the transfer function of the first **sub - network** (N1) with respect to the network parameters (a), in that the second gating function is equal to the gradient of the transfer function of the first **sub - network** (N1) with respect to the signals (c) delayed by the second **sub - network** , and in that the internal signals are equal to the gradient of the signals (d) output to the second **sub - network** (N2) by the first **sub - network** (N1) with respect to the network parameters (a).

(Dwg.1/7

Abstract (Equivalent): US 5111418 A

The network includes a first **subnetwork** having only delay free elements, being acted upon by input signals and emitting output signals, and a second **subnetwork** having only time lag elements, receiving signals from the first **subnetwork** and feeding back the signals with a delay to the first **subnetwork** . Further output signals are each formed corresponding to the gradient of the output signals with respect to the network **parameters** . The further **output** signals are equal to the sum of all of the signals produced by linking all of hte input signals, all of the signals delayed b the second **subnetwork** and all of the network parameters through a first linking function, and of all of the signals being a result of the linkage of all of the input signals, all of the signals delayed by the second **subnetwork** , and all of the network parameters through a second linking function multiplied by internal signals being delayed in accordance with the second **subnetwork** . The first linking function is equal to the gradient of a transfer function of the first **subnetwork** with respect to the network parameters. USE - A method and network configuration to obtain a gradient of output signals of a network for processing discrete time signals with respect to network parameters.

Title Terms: DERIVATIVE; GRADIENT; ADAPT; DIGITAL; SIGNAL; NETWORK; SUM; INPUT; SIGNAL; DELAY; SIGNAL; MULTIPLICATION; INTERNAL; SIGNAL

Derwent Class: U22; U25

International Patent Class (Main): H03H-021/00

International Patent Class (Additional): G06F-015/31

File Segment: EPI

Manual Codes (EPI/S-X): U22-G; U25-A02

13/9/14 (Item 14 from file: 350)

004255476
WPI Acc No: 1985-082354/198514
XRPX Acc No: N85-061726

Integrated circuit for digital filter - has subtractors and delay lines for luminance channel of colour TV receiver

Patent Assignee: DEUT ITT IND GMBH (INTT)
Inventor: BAKER P

Number of Countries: 008 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 135599	A	19850403	EP 83109517	A	19830924	198514	B
AU 8433323	A	19850328				198520	
JP 60089174	A	19850520	JP 84196957	A	19840921	198526	
US 4635119	A	19870106	US 84654635	A	19840924	198704	
EP 135599	B	19870708				198727	
DE 3372433	G	19870813				198733	

Priority Applications (No Type Date): EP 83109517 A 19830924
Cited Patents: 2.Jnl.Ref
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 135599	A	G	14		
Designated States (Regional): DE FR GB IT NL					
EP 135599	B	G			
Designated States (Regional): DE FR NL					

Abstract (Basic): EP 135599 A

The circuit has a second subcircuit (t2) containing a second series circuit comprising a third and fourth subcircuit (t3,t4) each comprising a third (and fourth) delay line (v3 etc.) and a first (and second) subtractor (s1,s2) whose one input receives the undelayed signal and whose other input receives the delayed signal from the third (and fourth) subcircuit.

The summer is a third subtractor (s3) whose one input is connected to the output of the multiplier (m) and whose other input is connected to the output of the second delay line. The delay time of all delay lines is equal to one clock period.

ADVANTAGE - No multiplier is needed for amplitude equalisation.

1/6

Abstract (Equivalent): EP 135599 B

Integrated circuit of a digital filter used in the digital luminance channel of a colour-television receiver to give image enhancement (peaking) and containing a first cascade of **subnetworks** the first of which (t1) consists of a first delay element (v1,v1') and a first adder (a1) for the input and output signals of the first delay element, and the second of which (t2) consists of a second delay element (v2,v2'), a multiplier (m) one input signal of which is a factor determining the measure of the image enhancement , and a summer which delivers the output signal of the digital filter and whose first and second inputs are connected to the output of the second delay element (c2,v2') and to the output of the multiplier (m), respectively, the delay provided by each of the delay elements being equal to an integral multiple of the period of the clock signal of the digital filter, whose frequency is equal to four times the chrominance-subcarrier frequency, characterised by the following features: The second **subnetwork** (t2) further includes a second formed by a third **subnetwork** (t3) and a fourth **subnetwork** (t4), the third **subnetwork** consisting of a third delay element (v3,v3') and a first

subtracter (s1), and the fourth **subnetwork** consisting of a fourth delay element (v4,v4') and a second subtracter (s2), the minuend inputs of said subtracters being fed with the undelayed signals of the third **subnetwork** and the fourth **subnetwork** , respectively, and the subtrahend inputs of said subtracters being fed with the delayed signals of the third **subnetwork** and the fourth **subnetwork** , respectively; The summer is a third subtracter (s3) having its subtrahend input and its minuend input connected to the output of the multiplier (m) and to the output of the second delay element (v2,v2'), respectively, and the delay provided by each of the first to fourth delay elements (v1-v4) is equal to one period of the clock signal of the digital filter. (7pp)

Abstract (Equivalent): US 4635119 A

The integrated circuit includes two cascaded **subnetworks** . One **subnetwork** includes a delay element and an adder at the input end of the digital filter. The output of the adder is coupled to the inputs of two further delay elements and to the minuend input of a subtracter.

The subtracter has its output connected to the input of a further delay element and to the subtrahend input of another subtracter. The output of this subtracter is coupled through a multiplier to the subtrahend input of a subtracter whose minuend input is connected to the output of the other delay element. The output of this subtracter is the digital filter **output** . The peaking **factor** is applied to the multiplier.

ADVANTAGE - Reduces required number of multipliers. (6pp

Title Terms: INTEGRATE; CIRCUIT; DIGITAL; FILTER; SUBTRACT; DELAY; LINE; LUMINOUS; CHANNEL; COLOUR; TELEVISION; RECEIVE

Derwent Class: U13; U22; W03

International Patent Class (Additional): H03H-017/02; H04N-005/20; H04N-009/64

File Segment: EPI

Manual Codes (EPI/S-X): U13-C; U22-G; W03-A05

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File 348:EUROPEAN PATENTS 1978-2005/Jan W02
         (c) 2005 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20050113,UT=20050106
         (c) 2005 WIPO/Univentio
File 324:German National Patents 1980-2004/Nov
         (c) 2004 Univentio

Set     Items   Description
S1       5801   SUBNET? OR SUB()(NET OR NETS OR NETWORK?)
S2     540098   NETWORK? OR NET OR NETS
S3        668   S1(3N)(PORTION? OR SECTION? OR PART OR PARTS OR DIVID? OR -
                SUBSET? OR SEGMENT? OR SUBDIVID? OR SUBDIVISION? OR DIVISION?
                OR REGION?)
S4        411   S1(3N)(SECTOR? ? OR ZONE? ? OR PARTIAL OR BRANCH? OR PARTI-
                TION? OR SUB()SET? ? OR AREA? ?)
S5        103   S1(3N)(COMPONENT? OR SUBCOMPONENT?)
S6    2361484   OUTPUT? OR OUT()(PUT??? ? OR PUTT??? ?) OR RESULT?
S7          1   S5(2W)FUNCTION? ?
S8     258579   S6:S7(5N)(PARAMETER? OR VARIABLE? OR ATTRIBUTE OR ATTRIBUT-
                ES OR VALUE OR VALUES OR FACTOR? ? OR FEATURE OR FEATURES)
S9     431477   IC OR ICS OR INTEGRATED(1W)CIRCUIT? OR MICROCIRCUIT? OR CH-
                IP? ? OR MICROCHIP? OR ICC OR ICCS
S10     20741   SIM OR SIMS OR SIMM OR SIMMS OR SINGLE(2W)MEMOR??? ?()MODU-
                LE? ?
S11    126275   CARD OR CARDS OR SMARTCARD? OR ATMCARD? OR CHIPCARD? OR IN-
                TELLIGENTCARD? OR DEBITCARD? OR CHARGECARD? OR CREDITCARD? OR
                CASHCARD? OR IDENTICARD?
S12       495   DATACARD? OR ICCARD? OR BANKCARD? OR MONEYCARD? OR FINANCE-
                CARD? OR TRANSACTIONCARD? OR PROCESS?RCARD? OR MICROPROCESS?R-
                CARD? OR MULTICARD?
S13       143   MEMOCARD? OR MEMORYCARD?
S14     18423   S6(2W)FUNCTION? ?
S15      1553   S14(5N)(PARAMETER? OR VARIABLE? OR ATTRIBUTE OR ATTRIBUTES
                OR VALUE OR VALUES OR FACTOR? ? OR FEATURE OR FEATURES)
S16         2   S15(20N)(S1 OR S3:S5)
S17    258579   S6(5N)(PARAMETER? OR VARIABLE? OR ATTRIBUTE OR ATTRIBUTES -
                OR VALUE OR VALUES OR FACTOR? ? OR FEATURE OR FEATURES)
S18        38   S17(20N)(S1 OR S3:S5)
S19         0   S18(20N)S9:S13
S20     52449   IC='G06F-017'
S21      6816   IC='G06F-007'
S22         4   S18 AND S20:S21
S23         5   S16 OR S22
S24         5   IDPAT (sorted in duplicate/non-duplicate order)
S25         5   IDPAT (primary/non-duplicate records only)

 25/5,K/1     (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2005 WIPO/Univentio. All rts. reserv.

01049668    **Image available**
METHOD AND APPARATUS FOR SYNTHESIS
PROCEDE ET DISPOSITIF DE SYNTHESE
Patent Applicant/Assignee:
  CADENCE DESIGN SYSTEMS INC, 2655 Seely Avenue, San Jose, CA 95134, US, US
    (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
  TEIG Steven, 935 College Avenue, Menlo Park, CA 94025, US, US (Residence)
    , US (Nationality), (Designated only for: US)
  ASMUS Hetzel, Blankenhainer Strasse 8a, 12249 Berlin, DE, DE (Residence),
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DE (Nationality), (Designated only for: US)
Legal Representative:
ADELI Mani (agent), Stattler Johansen & Adeli LLP, P.O. Box 51860, Palo Alto, CA 94303-0728, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200377630 A2-A3 20030925 (WO 0377630)
Application: WO 2003US2984 20030131 (PCT/WO US03002984)
Priority Application: US 200261459 20020131; US 200262014 20020131; US 200262044 20020131; US 200262017 20020131
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT SE SI SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-017/50**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 28366

English Abstract
A method for pre-tabulating sub-networks. This method (1) generates a sub-network that performs a function (605), (2) generates a parameter based on this function (610), and (3) stores the sub-network in a storage structure based on the generated parameters (635).

French Abstract
Dans certains de ses modes de realisation, cette invention concerne un procede de pre-tabulation de sous-reseaux. Ce procede consiste a: (1) creer un sous-reseau auquel est devolue une fonction; (2) generer un parametre selon cette fonction; et (3) stocker le sous-reseau dans une base a structure de stockage en fonction du parametre genere. Dans d'autres modes de realisation, le sous-reseau cree comporte plusieurs elements de circuit. Dans d'autres modes de realisation encore, le sous-reseau genere s'acquitte d'un ensemble d'au moins deux fonctions. Autres modes de realisation : stockage de chacun des sous-reseaux genere sous forme codee. Dans certains cas, l'invention peut concerner la description d'un mode de conception en termes de circuits. Autres modes de realisation encore : le procede (1) consiste a selectionner un sous-reseau dans un modele de conception, (2) identifier une fonction de sortie executee par le sous-reseau, (3) a partir de la fonction de sortie identifiee, reperer un sous-reseau de rechange dans la structure de stockage des sous-reseaux ; et dans certaines conditions, (4) remplacer le sous-reseau candidat selectionne par le sous-reseau de rechange repere. Dans certains modes de realisation, on reporte un modele dans une banque technologique particuliere. Selon certains modes de realisation, on trouve une structure de stockage de donnees dans laquelle est stockee une pluralite de sous-reseaux selon des parametres tires de leurs fonctions de sortie.

Legal Status (Type, Date, Text)
Publication 20030925 A2 Without international search report and to be

republished upon receipt of that report.
Examination 20040115 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20040325 Late publication of international search report
Republication 20040325 A3 With international search report.

Main International Patent Class: **G06F-017/50**
Fulltext Availability:
Detailed Description
Claims

Detailed Description
... mentioned above, when the indexer has to generate multiple indices (i.e., when the candidate **sub - network** , performs several **output functions**), the indexer selects an input **variable** configuration as the basis for the indices. This selection is further described below in Section...is dependent on all input variables). For instance, the process 900 could deal with candidate **sub - networks** that do not have an **output function** dependent on all input **variables** , by terminating its search for replacement **sub - networks** . Alternatively, the process 900 could deal with multi-function queries that do not have pivot...a pivot output function. Even though each generated graph has a pivot node, the resulting **sub - networks** might not have pivot functions because some of the input **variables** might drop out as a **result** of the particular functions implemented by the **sub - networks** .

The process also discards a **sub - network** when the **sub - network** has at least one node with an output that is not dependent on all the...

Claim
... function, and a plurality of the subnetworks perform more than one output function, wherein each **sub - network** outputs the result of each output function;
b) for each **sub - network** , generating a **parameter** based on the set of **output function** performed by the **sub - network** ;
c) storing each **sub - network** in a storage structure based on the parameter generated for the sub-network.

41 A...circuit description of a design, the method comprising: a) from the design, selecting a candidate **sub - network** that includes multiple circuit
elements;
b) generating a **parameter** based on a set of **output functions** performed by the
selected candidate **sub - network** ;
c) using the parameter to retrieve a replacement **sub - network** from a ...selecting a candidate sub-network that performs a set of output functions, wherein the candidate **sub - network** includes a set of circuit elements;
b) generating a **parameter** based on the set of **output functions** ;
c) using the **parameter** to retrieve a replacement **sub - network** from a storage structure
that stores replacement **sub - networks** ;
d) replacing the selected candidate **sub - network** with the replacement sub-network in the design.

64 The method of claim 63, wherein...
? t25/5,k/2,4;t25/6/5

25/5,K/2 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00855415 **Image available**

A METHOD AND SYSTEM FOR PERFORMING PERMUTATIONS USING PERMUTATION INSTRUCTIONS BASED ON MODIFIED OMEGA AND FLIP STAGES

PROCEDE ET SYSTEME POUR EFFECTUER DES PERMUTATIONS AU MOYEN D'INSTRUCTIONS DE PERMUTATION BASEES SUR UN ETAGE OMEGA ET UN ETAGE COMMUTE MODIFIES

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Patent Applicant/Inventor:
LEE Ruby B, 55 Ettl Circle, Princeton, NJ 08540, US, US (Residence), US (Nationality)
Legal Representative:
DUNN MCKAY Diane (agent), Mathews, Collins, Shepherd & Gould, P.A., Suite 306, 100 Thanet Circle, Princeton, NJ 08540, US,

Patent and Priority Information (Country, Number, Date):
Patent: WO 200189131 A2-A3 20011122 (WO 0189131)
Application: WO 2001US14535 20010507 (PCT/WO US0114535)
Priority Application: US 2000202243 20000505
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE
ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT
LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM
TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-007/38**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 13893

English Abstract
The present invention provides permutation instructions which can be used in software executed in a programmable processor (14) for solving permutation problems in cryptography, multimedia and other applications. The permute instructions are based on an omega-flip network comprising at least two stages in which each stage can perform the function of either an omega network stage or a flip network stage. Intermediate sequences of bits are defined that an initial sequence of bits from a source register are transformed into. Each intermediate sequence of bits is used as input to a subsequent permutation instruction. Permutation instructions are determined for permuting the initial source sequence of bits into one or more intermediate sequence of bits until a desired sequence is obtained. The intermediate sequences of bits are determined by configuration bits.

French Abstract
La presente invention concerne des instructions de permutation qui peuvent etre utilisees dans un logiciel execute dans un processeur programmable pour regler des problemes de permutation dans des applications de cryptographie, multimedia ou autres. Ces instructions de permutation sont basees sur un reseau omega-commute comprenant au moins deux etages dont chacun peut remplir la fonction d'un etage omega ou d'un

etage commute. Des sequences de bits intermediaires sont definies dans lesquelles une sequence de bits initiale provenant d'un registre source est transformee. Chaque sequence de bits intermediaire est utilisee comme donnees d'entrée pour une instruction de permutation subsequente. Les instructions de permutation sont determinees afin de permuter la sequence de bits source initiale en une ou plusieurs sequences de bits intermediaires jusqu'a ce qu'une sequence desiree soit obtenue. Les sequences de bits intermediaires sont determinees par des bits de configuration. Les instructions de permutation forme une sequence d'instructions de permutation comprenant au moins une instruction. Des instructions de permutation d'au plus 21 gr/m sont utilisees dans la sequence d'instructions de permutation (r etant le nombre de sous-mots a k-bits devant etre permutes; m etant le nombre d'etages du reseau executes dans une instruction). Les instructions de permutation peuvent etre utilisees pour permuter des sous-mots a k-bits mis en paquets dans un mot a n-bits (k pouvant etre 1, 2,... ou n bits; et k"sup"*r=n).

Legal Status (Type, Date, Text)
Publication 20011122 A2 Without international search report and to be republished upon receipt of that report.
Search Rpt 20020613 Late publication of international search report
Republication 20020613 A3 With international search report.
Republication 20020613 A3 Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

Main International Patent Class: G06F-007/38
Fulltext Availability:
Detailed Description
Detailed Description
... inputs" have already been configured, go to Step 4.

2a. Connect "current input" to the **sub - network** "sub 1 " that is on the same side as "current input". Connect the **output** that has the same **value** as "current input", to sub 1 and call it "output (current input)". Set "current outpuf...

...of "output (current input)" and go to Step 3.

2b. Connect "current input" to the **sub - network** "sub 1 " such that "sub 1 " is not '4 sub2".

Connect the **output** that has the same **value** as "currentinpuC, to sub 1 and call it "output (current input)". Set "current outpuf' to the conflict output of "output (current input)".

3 . Connect "current outpuV to **sub - network** "sub2" such that "subT' is not "sub 1". Also connect the input that has the same **value** as "current **output** ", call it "input (current output)", to G 4sub2". If "input (current output)" is the same...and its conflict input, node 152 as "end inpuf'. Node 151 is connected to the **subnet** 156 that is on the same side as node 151. The **output** that has the **value** a is node 153. It is marked as "output (current input)". Node 153 is connected to **subnet** 156, which is the sarne subnet as node 151 is connected to. The conflict output...

25/5,K/4 (Item 4 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00367144 **Image available**

APPARATUS AND METHOD FOR MODELING LINEAR AND QUADRATIC PROGRAMS

APPAREIL ET PROCEDE POUR MODELER DES PROGRAMMES LINEAIRES ET QUADRATIQUES

Patent Applicant/Assignee:
HAUSMAN Robert E,
LAWLIS Robert M,
Inventor(s):
HAUSMAN Robert E,
LAWLIS Robert M,

Patent and Priority Information (Country, Number, Date):
Patent: WO 9707471 A1 19970227
Application: WO 96US12988 19960809 (PCT/WO US9612988)
Priority Application: US 952232 19950811
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
CA JP RU AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-017/50**
International Patent Class: G06F-17:60
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 16820

English Abstract

An apparatus and method for modeling optimization problems providing variable specification of both input and output in enhanced graph theoretic form. Problem elements including nodes and links may be defined, as may constraints on nodes and links and on groups of nodes and links including proportional and required relationships between network elements and groups of network elements that are connected and unconnected. Data received in enhanced graph theoretic format are transformed into the form of an objective function, possibly including linear, bilinear, and quadratic terms, and a system of constraints, which are then solved using network program, linear program or mixed integer linear program software.

French Abstract

L'invention concerne un appareil et un procede pour modeler des problemes d'optimisation en fournissant des specifications variables de l'entree aussi bien que de la sortie, sous forme theorique graphique amelioree. Les elements de problemes comprenant des noeuds et des liaisons peuvent etre definis, de meme que des contraintes sur des noeuds et des liaisons et sur des groupes de noeuds et de liaisons comprenant des relations proportionnelles et requises entre des elements de reseau et des groupes d'elements de reseau qui sont connectes et deconnectes. Les donnees recues en format theorique graphique ameliore sont transformees sous forme d'une fonction objective, comprenant, eventuellement, des termes lineaires, bilineaires et quadratiques et un systeme de contraintes qui sont ensuite resolues a l'aide d'un programme de reseau, d'un programme lineaire ou d'un logiciel de programme lineaire de nombres entiers mixtes.

Main International Patent Class: **G06F-017/50**
Fulltext Availability:
Detailed Description

Detailed Description

... above) for solution.

The solution values are then transformed by software (called NETRPT) into a **subnetwork** of the original model graph. The **output values** reside in a file or memory store *.RPT, and may be fed into NETWK for...

```
File   6:NTIS 1964-2005/Jan W2
         (c) 2005 NTIS, Intl Cpyrght All Rights Res
File   2:INSPEC 1969-2005/Jan W2
         (c) 2005 Institution of Electrical Engineers
File   8:Ei Compendex(R) 1970-2005/Jan W2
         (c) 2005 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2005/Jan W2
         (c) 2005 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2004/Dec
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2005/Jan W3
         (c) 2005 BLDSC all rts. reserv.
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         (c)2005 Japan Science and Tech Corp(JST)
File  95:TEME-Technology & Management 1989-2004/Jun W1
         (c) 2004 FIZ TECHNIK
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Nov
         (c) 2004 The HW Wilson Co.
File 111:TGG Natl.Newspaper Index(SM) 1979-2005/Jan 13
         (c) 2005 The Gale Group
File 144:Pascal 1973-2005/Jan W2
         (c) 2005 INIST/CNRS
File 256:TecInfoSource 82-2004/Dec
         (c) 2004 Info.Sources Inc
File 266:FEDRIP 2004/Oct
         Comp & dist by NTIS, Intl Copyright All Rights Res
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File 483:Newspaper Abs Daily 1986-2005/Jan 17
         (c) 2005 ProQuest Info&Learning
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
File 603:Newspaper Abstracts 1984-1988
         (c)2001 ProQuest Info&Learning

Set     Items   Description
S1       9534   SUBNET? OR SUB()(NET OR NETS OR NETWORK?)
S2    3426431   NETWORK? OR NET OR NETS
S3        420   S1(3N)(PORTION? OR SECTION? OR PART OR PARTS OR DIVID? OR -
                SUBSET? OR SEGMENT? OR SUBDIVID? OR SUBDIVISION? OR DIVISION?
                OR REGION?)
S4        399   S1(3N)(SECTOR? ? OR ZONE? ? OR PARTIAL OR BRANCH? OR PARTI-
                TION? OR SUB()SET? ? OR AREA? ?)
S5         72   S1(3N)(COMPONENT? OR SUBCOMPONENT?)
S6   13977284   OUTPUT? OR OUT()(PUT??? ? OR PUTT??? ?) OR RESULT?
S7      20644   S6(2W)FUNCTION? ?
S8     536593   S6(5N)(PARAMETER? OR VARIABLE? OR ATTRIBUTE OR ATTRIBUTES -
                OR VALUE OR VALUES OR FACTOR? ? OR FEATURE OR FEATURES)
S9          9   S7 AND (S1 OR S3:S5)
S10       109   S8 AND (S1 OR S3:S5)
S11    991835   IC OR ICS OR INTEGRATED(1W)CIRCUIT? OR MICROCIRCUIT? OR CH-
                IP? ? OR MICROCHIP? OR ICC OR ICCS
S12     81783   SIM OR SIMS OR SIMM OR SIMMS OR SINGLE(2W)MEMOR??? ?()MODU-
                LE? ?
S13    235566   CARD OR CARDS OR SMARTCARD? OR ATMCARD? OR CHIPCARD? OR IN-
                TELLIGENTCARD? OR DEBITCARD? OR CHARGECARD? OR CREDITCARD? OR
                CASHCARD? OR IDENTICARD?
S14       869   DATACARD? OR ICCARD? OR BANKCARD? OR MONEYCARD? OR FINANCE-
                CARD? OR TRANSACTIONCARD? OR PROCESS?RCARD? OR MICROPROCESS?R-
                CARD? OR MULTICARD?
S15        21   MEMOCARD? OR MEMORYCARD?
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S16          4   S10 AND S11:S15
S17         13   S9 OR S16
S18          0   S17/2002:2005
S19          7   RD S17 (unique items)
S20         20   AU='TEIG S':AU='TEIG SL'
S21         20   AU='TEIG, S.':AU='TEIG, STEVEN L.'
S22          4   AU='HETZEL A D':AU='HETZEL AJ'
S23         25   AU='HETZEL, A':AU='HETZEL, A.J.'
S24          1   AU='HETZEL, ASMUS'
S25          0   TEIG(2N)STEV?
S26          0   HETZEL(2N)ASMUS
S27         70   S20:S24
S28          0   S27 AND S7:S8
S29          0   S27 AND (S1 OR S3:S5)
?
```

19/7/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6082480 INSPEC Abstract Number: C9812-7445-020
Title: A mixed integer linear programming model for dynamic route guidance
Author(s): Kaufman, D.E.; Nonis, J.; Smith, R.L.
Author Affiliation: AT&T Labs., Somerset, NJ, USA
Journal: Transportation Research, Part B (Methodological) vol.32B, no.6 p.431-40
Publisher: Elsevier,
Publication Date: Aug. 1998 Country of Publication: UK
CODEN: TRBMDY ISSN: 0191-2615
SICI: 0191-2615(199808)32B:6L.431:MILP;1-P
Material Identity Number: T204-98004
U.S. Copyright Clearance Center Code: 0191-2615/98/$19.00+0.00
Document Number: S0191-2615(98)00013-7
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: One of the major challenges facing ITS (intelligent transportation systems) today is to offer route guidance to vehicular traffic so as to reduce trip time experienced. In a cooperative route guidance system, the problem becomes one of assigning routes to vehicles departing at given times from a set of origins to a set of destinations so as to minimize the average trip time experienced (a system optimal criterion). Since the time to traverse a link will depend upon traffic volume encountered on that link, link times are dynamic. The complex interaction **resulting** between objective **function** and constraints makes the dynamic problem significantly more difficult to formulate and solve than the static version. We present a mixed integer linear programming formulation of the problem which is formally derived from a set of traffic flow assumptions. Principal among these is the simplifying assumption that vehicles upon entering a link, assume the speed that traffic would attain were the traffic volume encountered on that link in steady-state. The integer variables correspond to selection of vehicle capacity constraints on the link while the continuous variables correspond to selection of vehicle routes. Implicit within this MILP formulation of the dynamic traffic assignment problem is therefore a decomposition of the problem which results in a conventional capacitated linear programming network flow problem. A small illustrative **subnetwork** extracted from the city of Sioux Falls is solved to optimality by IBM's OSL branch-and-bound algorithm. (21 Refs)
Subfile: C

19/7/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

04136719 INSPEC Abstract Number: B9206-1160-003
Title: An approach to the analysis of nonlinearly terminated black-box circuits based on polynomial congruence techniques
Author(s): Calandra, E.F.; Sommariva, A.M.
Author Affiliation: Dept. of Electr. Eng., Palermo Univ., Italy
Conference Title: Proceedings of the 33rd Midwest Symposium on Circuits and Systems (Cat. No.90CH2819-1) p.885-8 vol.2
Editor(s): Johnston, R.H.; Nowrouzian, B.; Turner, L.E.
Publisher: IEEE, New York, NY, USA
Publication Date: 1991 Country of Publication: USA 2 vol. 1205 pp.
ISBN: 0 7803 0081 5

U.S. Copyright Clearance Center Code: CH2819-1/90/0000-0885$01.00
Conference Sponsor: IEEE
Conference Date: 12-14 Aug. 1990 Conference Location: Calgary, Alta., Canada
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: An approach to the problem of deriving the overall dynamical model of an electrical circuit containing a linear lumped time-invariant black-box network terminated by nonlinear elements (with or without memory) and driven by independent signal sources, is presented. Extensive use is made of polynomial congruence techniques of number theory to determine a nonredundant set of differential equations in the nonlinear port variables and then the set of algebraic dynamical transfer relationships expressing **output** variables as **functions** of the integration ones, source signals, and their derivatives. The two-step procedure devised rests on extensive use of polynomial congruence techniques, which allows one to derive the polynomial operators appearing in the system differential equations by simple algebraic manipulations of the linear **sub - network** matrices. This feature makes the method particularly attractive for computer-assisted design applications, especially in the case of high-frequency circuits, for which a modular black-box approach based on measurement data is often desirable or even required. (8 Refs)
Subfile: B

19/7/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

03229972 INSPEC Abstract Number: B88063625, C88057178
Title: A method of fault analysis for test generation and fault diagnosis
Author(s): Cox, H.; Rajski, J.
Author Affiliation: Dept. of Electr. Eng., McGill Univ., Montreal, Que., Canada
Journal: IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems vol.7, no.7 p.813-33
Publication Date: July 1988 Country of Publication: USA
CODEN: ITCSDI ISSN: 0278-0070
U.S. Copyright Clearance Center Code: 0278-0070/88/0700-0813$01.00
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Theoretical (T)
Abstract: The authors present a fault coverage analysis method for test generation and fault diagnosis of large combinational circuits. Input vectors are analyzed in pairs in two steps using a 16-valued logic system, GEMINI. Forward propagation is performed to determine, for each line in the network, the set of all possible values it can take if the network contains any single or multiple faults. Based on the **values** observed at primary **outputs** , backward implication is performed to determine the value actually carried by each line. Some deduced values imply the line is not faulty; similarly, some values imply that there is a fault in the **subnetwork** driving the line, or on the line itself. By keeping track of this information, it is possible to locate a fault to within its equivalence class. An extended fault model which includes stuck-at, stuck-open, and delay faults is used. Multiple faults of all multiplicities are implicitly considered; thus, the results obtained using this method are not invalidated in the presence of untested or untestable lines. (22 Refs)
Subfile: B C

19/7/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

03044773 INSPEC Abstract Number: C88007006
Title: Behavioral specification of state machine networks by event sequences
Author(s): Yamanouchi, N.
Author Affiliation: Tokyo Res. Lab., IBM Japan Ltd., Japan
Journal: Transactions of the Institute of Electronics, Information and Communication Engineers D vol.J70D, no.8 p.1453-61
Publication Date: Aug. 1987 Country of Publication: Japan
CODEN: DJTDE2 ISSN: 0374-468X
Language: Japanese Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: A behavioral description method of state machine networks is explored. The method, based on the input- **output** sequence mapping **functions** by Kahn and augmented by the output-input cross-timing enables one to specify behavior of state machines including those with bounded input buffering capacity. A model of network composition from **subnetworks** is also proposed so that the network behavior description is composed from the behavior of the **subnetworks** . The composition model, an algebra with three composition operators is shown to be complete to guarantee that behavior of any reasonable network is composed from those of element modules. (17 Refs)
Subfile: C

19/7/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

02758591 INSPEC Abstract Number: B86063458
Title: Segmented waveform relaxation algorithms for large scale circuit simulation
Author(s): Dumlugol, D.; Cockx, J.; De Man, H.; Odent, P.
Author Affiliation: Dept., Elektrotech., Katholieke Univ., Leuven, Heverlee, Belgium
Conference Title: 1985 International Symposium on Circuits and Systems. Proceedings (Cat. No.85CH2114-7) p.1069-72 vol.3
Publisher: IEEE, New York, NY, USA
Publication Date: 1985 Country of Publication: USA 3 vol. 1704 pp.
U.S. Copyright Clearance Center Code: CH2114-7/85/0000-1069$01.00
Conference Sponsor: IEEE; IECE (Japan)
Conference Date: 5-7 June 1985 Conference Location: Kyoto, Japan
Availability: IEEE Service Center, Piscataway, NJ, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: New algorithms are presented for computation of accurate starting and relaxed waveforms with the waveform relaxation method (WRM) for circuit simulation of MOS circuits. Accurate starting waveforms are of great importance since WRM has linear convergence. Simulation of feedback loops constitutes the major problem. The novelty of the algorithms proposed consists in the application of logic simulation techniques together with time segmentation and dynamic leveling of **subnetworks** to compute starting waveforms. The latter scheme is a powerful alternative to static leveling which simulates **subnetworks** in a fixed order. The new algorithms show great potential for applicability on multimicroprocessor computers and for interactive circuit simulation. A new circuit simulator, SWAN, has been developed on the basis of these algorithms. Test results on large circuits with SWAN show a speed increase of a **factor** of 50 over SPICE, **resulting** in accurate starting waveforms. Relaxed waveforms are obtained more than 10

times faster than with SPICE for large circuits. (8 Refs)
Subfile: B

19/7/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

01877942 INSPEC Abstract Number: B82034203
Title: A novel approach to test generation for VLSI
Author(s): Timoc, C.; Stott, F.; Hess, L.
Conference Title: Digest of Papers Spring COMPCON 82. High Technology in the Information Industry p.78-86
Publisher: IEEE, New York, NY, USA
Publication Date: 1982 Country of Publication: USA xvi+418 pp.
Conference Sponsor: IEEE
Conference Date: 22-25 Feb. 1982 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: A new family of custom **integrated circuits** called microsimulators was developed and fabricated to aid test generation and design verification of very large scale **integrated circuits** . The microsimulators are aiding design verification by isolating a **subnetwork** from a network, forcing the inputs of the **subnetwork** to any logic **value** , and monitoring the **outputs** of the **subnetwork** for measuring verification comprehensiveness. Test generation is performed with the aid of the microsimulators by automatically injecting three types of faults viz. stuck-at, stuck-open, and bridging. A simulator of a commercially available microprocessor was implemented with microsimulators and used to develop test vectors. The test set was minimized and presently it comprises 14000 vectors detecting 99.7% of the single stuck-at faults. Work is in progress to develop test vectors for stuck-open and bridging faults. It is apparent from this experimental work that simulation implemented in hardware is at least one order and possibly two orders of magnitude more cost-effective than software simulation. (12 Refs)
Subfile: B

19/7/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

01723622 INSPEC Abstract Number: B81036172, C81026058
Title: Synthesis of multiple-output combinational networks using multiplexors
Author(s): Butov, A.A.
Journal: Kibernetika vol.16, no.3 p.63-70
Publication Date: May-June 1980 Country of Publication: USSR
CODEN: KBRNA5 ISSN: 0023-1274
Translated in: Cybernetics vol.16, no.3 p.375-83
Publication Date: May-June 1980 Country of Publication: USA
CODEN: CYBNAW ISSN: 0011-4235
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: The synthesis method of combinational circuits described is a development of Shannon's method (1963) and Povarov's cascade method (1957). It realizes a system of completely determined Boolean functions F=(f/sub 0/,f/sub 1/,...,f/sub m-1/) which depend on variables from the set X=(x/sub 1/,x/sub 2/,...,x/sub n/) by a logic network of multiplexors and

low-integration elements (the corresponding **subnetworks** are called mu -networks and lambda -networks, respectively). According to the basic approach of this method, coefficients in the expansion of the functions from F which coincide up to inversion are realized only once. The expansion is realized using multiplexors, with the expansion variables on the control inputs and the expansion coefficients on the data inputs. The expansion is continued until the residual functions of the current system are independent of lambda variables, where lambda =(log/sub 2/(n+(log/sub 2/ m)-)log/sub 2/ n()), at which stage the low-integration elements are used to synthesize a lambda -network realizing the **resultant** system of **functions** . (5 Refs)

Subfile: B C

?

```
File 696:DIALOG Telecom. Newsletters 1995-2005/Jan 13
         (c) 2005 The Dialog Corp.
File  15:ABI/Inform(R) 1971-2005/Jan 17
         (c) 2005 ProQuest Info&Learning
File  98:General Sci Abs/Full-Text 1984-2004/Sep
         (c) 2004 The HW Wilson Co.
File 112:UBM Industry News 1998-2004/Jan 27
         (c) 2004 United Business Media
File 141:Readers Guide 1983-2004/Sep
         (c) 2004 The HW Wilson Co
File 484:Periodical Abs Plustext 1986-2005/Jan W2
         (c) 2005 ProQuest
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         (c)2005 Knight Ridder/Tribune Bus News
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File 613:PR Newswire 1999-2005/Jan 13
         (c) 2005 PR Newswire Association Inc
File 635:Business Dateline(R) 1985-2005/Jan 15
         (c) 2005 ProQuest Info&Learning
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 610:Business Wire 1999-2005/Jan 18
         (c) 2005 Business Wire.
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         (c) 2005 Reed Business Information Ltd.
File 370:Science 1996-1999/Jul W3
         (c) 1999 AAAS
File  20:Dialog Global Reporter 1997-2005/Jan 18
         (c) 2005 The Dialog Corp.
File 624:McGraw-Hill Publications 1985-2005/Jan 18
         (c) 2005 McGraw-Hill Co. Inc
File 634:San Jose Mercury  Jun 1985-2005/Jan 17
         (c) 2005 San Jose Mercury News
File 647:CMP  Computer Fulltext 1988-2005/Jan W1
         (c) 2005 CMP Media, LLC
File 674:Computer News Fulltext 1989-2005/Jan W2
         (c) 2005 IDG Communications

Set     Items   Description
S1       7513   SUBNET? OR SUB()(NET OR NETS OR NETWORK?)
S2    8540011   NETWORK? OR NET OR NETS
S3        345   S1(3N)(PORTION? OR SECTION? OR PART OR PARTS OR DIVID? OR -
              SUBSET? OR SEGMENT? OR SUBDIVID? OR SUBDIVISION? OR DIVISION?
              OR REGION?)
S4        163   S1(3N)(SECTOR? ? OR ZONE? ? OR PARTIAL OR BRANCH? OR PARTI-
              TION? OR SUB()SET? ? OR AREA? ?)
S5         25   S1(3N)(COMPONENT? OR SUBCOMPONENT?)
S6   10801399   OUTPUT? OR OUT()(PUT??? ? OR PUTT??? ?) OR RESULT?
S7       3229   S6(2W)FUNCTION? ?
S8     809738   S6(5N)(PARAMETER? OR VARIABLE? OR ATTRIBUTE OR ATTRIBUTES -
              OR VALUE OR VALUES OR FACTOR? ? OR FEATURE OR FEATURES)
S9          1   S7(S)(S1 OR S3:S5)
S10        30   S8(S)(S1 OR S3:S5)
S11        31   S9:S10
S12         7   S11/2002:2005
S13        24   S11 NOT S12
S14        22   RD (unique items)
S15         0   AU='TEIG S'
S16         0   AU='HETZEL A'
S17         0   AU=TEIG, S
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S18          0   AU='HETZEL, A'
S19         45   TEIG(2N)STEVE?
S20          0   HETZEL(2N)ASMUS
S21          0   S19 AND (S1 OR S3:S5)
S22          0   S19 AND S7:S8
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14/3,K/2 (Item 2 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

01896573 05-47565
Estimating the cost of change orders
Moselhi, Osama
Transactions of AACE International PP: ES21-ES25 1998
ISSN: 1074-7397 JRNL CODE: AEE
WORD COUNT: 2661

...TEXT: developed, including its suitability for neural networks. It is essential here to identify input and **output parameters** (i.e., the input buffer and output layer). The real numbers associated with input data...

...0. Depending on the size of the problem (i.e., the number of input and **output parameters**), either a single network or a number of **subnetworks** forming a super or a global network could be used. In either case, one may ...

14/3,K/6 (Item 6 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00463779 89-35566
A Declarative Neural Network Description Language
Korb, Thomas; Zell, Andreas
Microprocessing & Microprogramming v27n1-5 PP: 181-188 Aug 1989
ISSN: 0165-6074 JRNL CODE: EUJ

...ABSTRACT: and Structured Query Language (SQL). Units in NESILA can have any number of input and **output** connections and one **parameter** , the units activation. NESILA employs only a small set of keywords but provides a rich...

...types are integer and floating point numbers. NESILA also provides mechanisms to construct networks from **subnets** .

14/3,K/13 (Item 1 from file: 635)
DIALOG(R)File 635:Business Dateline(R)

0420186 93-72236
Xyplex announces shipment of Ethernet Switch, Repeaters
Fetterman, Patrick J
Business Wire (San Francisco, CA, US) s1 p1
PUBL DATE: 930809
WORD COUNT: 716
DATELINE: Littleton, MA, US

TEXT:

...matching the 206 with the appropriate processor module.

In the Network 9000 Routing Hub, input/ **output** (I/O) **functions** and processor functions reside on separate modules that made with the midplane communications bus from...

...port while jamming all other ports; and the 220 Hub/Router, which creates a network **segment** , or **subnet** , of all the ports on the attached concentrator. No other vendor offers the range of...

14/3,K/16 (Item 2 from file: 20)
DIALOG(R)File 20:Dialog Global Reporter

06539999 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Internet protocol (IP) network: Basic issues
HINDU
August 05, 1999
JOURNAL CODE: FHIN LANGUAGE: English RECORD TYPE: FULLTEXT
WORD COUNT: 3612

(USE FORMAT 7 OR 9 FOR FULLTEXT)

... 00001010 00000011 00001110
logical AND
11111111 11111111 11111111 00000000
equals
10000000 00001010 00000011 00000000

The **result** provides the **subnet** **value** of 172.16.3. You will notice that a **subnet** is normally identified as a concatenation of the network number and **subnet** number. The trailing zero is not normally shown. The original datagram can now be routed to its destination within the network based on its **subnet** value.

The subnet mask stated in the example uses the full 8 bits for the...

```
File   9:Business & Industry(R) Jul/1994-2005/Jan 14
         (c) 2005  The Gale Group
File  16:Gale Group PROMT(R) 1990-2005/Jan 17
         (c) 2005 The Gale Group
File  47:Gale Group Magazine DB(TM) 1959-2005/Jan 17
         (c) 2005 The Gale group
File 148:Gale Group Trade & Industry DB 1976-2005/Jan 17
         (c)2005 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 275:Gale Group Computer DB(TM) 1983-2005/Jan 17
         (c) 2005 The Gale Group
File 621:Gale Group New Prod.Annou.(R) 1985-2005/Jan 17
         (c) 2005 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2005/Jan 17
         (c) 2005 The Gale Group
File 649:Gale Group Newswire ASAP(TM) 2005/Jan 10
         (c) 2005 The Gale Group

Set     Items   Description
S1      13008   SUBNET? OR SUB()(NET OR NETS OR NETWORK?)
S2    9705663   NETWORK? OR NET OR NETS
S3        525   S1(3N)(PORTION? OR SECTION? OR PART OR PARTS OR DIVID? OR -
              SUBSET? OR SEGMENT? OR SUBDIVID? OR SUBDIVISION? OR DIVISION?
              OR REGION?)
S4        290   S1(3N)(SECTOR? ? OR ZONE? ? OR PARTIAL OR BRANCH? OR PARTI-
              TION? OR SUB()SET? ? OR AREA? ?)
S5         47   S1(3N)(COMPONENT? OR SUBCOMPONENT?)
S6    9168698   OUTPUT? OR OUT()(PUT??? ? OR PUTT??? ?) OR RESULT?
S7       5558   S6(2W)FUNCTION? ?
S8     989684   S6(5N)(PARAMETER? OR VARIABLE? OR ATTRIBUTE OR ATTRIBUTES -
              OR VALUE OR VALUES OR FACTOR? ? OR FEATURE OR FEATURES)
S9          0   S7(S)(S1 OR S3:S5)
S10        17   S8(S)(S1 OR S3:S5)
S11         3   S10/2002:2005
S12        14   S10 NOT S11
S13        10   RD (unique items)
S14         0   AU='TEIG S'
S15         1   AU='TEIG, STEVEN L.'
S16         0   AU=HETZEL, A
S17         0   AU='HETZEL, A'
S18        72   TEIG(2N)STEVE? OR HETZEL(2N)ASMUS
S19         0   S15:S18 AND S7:S8
S20         0   S15:S18 AND (S1 OR S3:S5)
```

13/3,K/7 (Item 1 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01340799 Supplier Number: 46098217 (USE FORMAT 7 FOR FULLTEXT)
Meta-Software Announces High-Performance Circuit Design and Simulation Control Environment that Increases Designer Productivity
News Release, pN/A
Jan 29, 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 757

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...simulation results. Users check the results that correspond only to the particular set of PVT **parameters** . The simulation **output** files are managed by a "makefile"-like facility. This facility minimizes the number of HSPICE or MetaCircuit jobs that have to be re-submitted when analysis **parameters** change. Only those **output** files which depend on the changed input parameters are regenerated. This feature increases the user...

...enabling the user to simulate only specific portions of the design. Users can also extract **subnets** from an HSPICE netlist without having to re-enter those paths on a new schematic...
?

File 347:JAPIO Nov 1976-2004/Aug(Updated 041203)
(c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2005/UD,UM &UP=200504
(c) 2005 Thomson Derwent
File 348:EUROPEAN PATENTS 1978-2005/Jan W02
(c) 2005 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20050113,UT=20050106
(c) 2005 WIPO/Univentio
File 324:German National Patents 1980-2004/Nov
(c) 2004 Univentio

Set	Items	Description
S1	83	AU=TEIG S?
S2	11	AU=HETZEL A?
S3	7651	SUBNET? OR SUB()(NET OR NETS OR NETWORK?)
S4	85	S1:S2
S5	5602797	OUTPUT? OR OUT()(PUT?? ? OR PUTT??? ?) OR RESULT?
S6	831	S3(20N)S5
S7	6	S4 AND S6

7/9/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015875445 **Image available**
WPI Acc No: 2004-033276/200403
XRPX Acc No: N04-026369
Technology mapping performing method, involves selecting candidate sub-network from design, and replacing selected candidate sub-network in design with replacement sub-network
Patent Assignee: HETZEL A (HETZ-I); TEIG S (TEIG-I)
Inventor: **HETZEL A** ; **TEIG S**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030217340	A1	20031120	US 200266456	A	20020131	200403	B

Priority Applications (No Type Date): US 200266456 A 20020131
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030217340	A1		48	G06F-017/50	

Abstract (Basic): US 20030217340 A1
NOVELTY - The method involves receiving a design that is not bounded to a particular technology. A candidate sub-network is selected from the design, and a replacement sub-network is identified from a storage structure that stores replacement sub-networks, which are bound to the technology. The selected candidate sub-network in the design is replaced with the identified replacement sub-network.
DETAILED DESCRIPTION - Some of the selected candidate **sub - networks** have multiple circuit portions that provide multiple **outputs** of the **sub - networks** . An INDEPENDENT CLAIM is also included for a computer program for receiving a design that is not bounded to a particular technology and for mapping the design to a particular technology.
USE - Used for performing technology mapping.
ADVANTAGE - The method effectively maps the design to a particular technology, and allows efficient storing and identification of multi-unit and/or multi-function sub-networks. The candidate sub-networks that are mapped to a particular technology do not need tree structures, but rather have more general directed acyclic graph

structures.
DESCRIPTION OF DRAWING(S) - The drawing shows a flowchart of a process of performance of an indexer manager.
pp; 48 DwgNo 9/26
Title Terms: TECHNOLOGY; MAP; PERFORMANCE; METHOD; SELECT; CANDIDATE; SUB; NETWORK; DESIGN; REPLACE; SELECT; CANDIDATE; SUB; NETWORK; DESIGN; REPLACE; SUB; NETWORK
Derwent Class: T01
International Patent Class (Main): G06F-017/50
File Segment: EPI
Manual Codes (EPI/S-X): T01-J15; T01-S03

7/9/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015875369 **Image available**
WPI Acc No: 2004-033200/200403
XRPX Acc No: N04-026293
Data storage structure for combinational logic synthesizer, stores each sub - network **in terms of graph and set of local functions, based on specific parameters derived from** output **function of** sub - network
Patent Assignee: HETZEL A (HETZ-I); TEIG S (TEIG-I)
Inventor: **HETZEL A ; TEIG S**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030217026	A1	20031120	US 200262992	A	20020131	200403 B

Priority Applications (No Type Date): US 200262992 A 20020131
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030217026	A1		48	G06F-007/00	

Abstract (Basic): US 20030217026 A1
NOVELTY - The data storage structure stores each sub- network in terms of a graph that represents the topology of set of integrated circuit element of each **sub - network** , and set of local functions for each node of the graph, based on specific parameters derived from **output** function of **sub - network** .
DETAILED DESCRIPTION - AN INDEPENDENT CLAIM is also included for sub-network record management system.
USE - Data storage structure for storing sub-network in combinational logic synthesizer for design of integrated circuit (IC).
ADVANTAGE - The data storage structure which efficiently stores **sub network** using specific parameters derived form **output** function of **sub network** is obtained.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of software architecture of logic synthesizer
network data storage (105)
global optimizer (110)
data generator (115)
timing engine (120)
designing unit (135)
pp; 48 DwgNo 1/26
Title Terms: DATA; STORAGE; STRUCTURE; COMBINATION; LOGIC; SYNTHESISER; STORAGE; SUB; NETWORK; TERM; GRAPH; SET; LOCAL; FUNCTION; BASED; SPECIFIC ; PARAMETER; DERIVATIVE; OUTPUT; FUNCTION; SUB; NETWORK
Derwent Class: T01; U11

International Patent Class (Main): G06F-007/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-J15A2; T01-N02A2; U11-G09

7/9/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015683552 **Image available**
WPI Acc No: 2003-745741/200370
XRPX Acc No: N03-597439
Technology mapping method for designing integrated circuit, involves replacing selected candidate sub-network in design with replacement sub-network
Patent Assignee: HETZEL A (HETZ-I); TEIG S (TEIG-I)
Inventor: **HETZEL A ; TEIG S**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030159115	A1	20030821	US 200262993	A	20020131	200370	B

Priority Applications (No Type Date): US 200262993 A 20020131
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030159115	A1		48	G06F-017/50	

Abstract (Basic): US 20030159115 A1
NOVELTY - A parameter for identifying a replacement **sub - network** that is bound to a 0.13 micron or 0.1 micron technology, is generated based on a set of **output** functions performed by selected candidate **sub - network** in the received design. The selected candidate **sub - network** is replaced with the identified replacement sub-network.
USE - For designing integrated circuit (IC).
ADVANTAGE - Enables superior mapping of networks that are not bound to any target library, to a particular target library.
DESCRIPTION OF DRAWING(S) - The figure shows a flowchart explaining replacement sub-network determination process.
pp; 48 DwgNo 14/26
Title Terms: TECHNOLOGY; MAP; METHOD; DESIGN; INTEGRATE; CIRCUIT; REPLACE; SELECT; CANDIDATE; SUB; NETWORK; DESIGN; REPLACE; SUB; NETWORK
Derwent Class: T01; U11
International Patent Class (Main): G06F-017/50
File Segment: EPI
Manual Codes (EPI/S-X): T01-J15A2; U11-G

7/9/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015683224 **Image available**
WPI Acc No: 2003-745413/200370
XRPX Acc No: N03-597126
Data storage structure, includes set of sub - networks that are stored based on set of indices derived from output functions of sub - networks
Patent Assignee: HETZEL A (HETZ-I); TEIG S (TEIG-I)
Inventor: **HETZEL A ; TEIG S**
Number of Countries: 001 Number of Patents: 001

Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 20030154210 A1 20030814 US 200261474 A 20020131 200370 B

Priority Applications (No Type Date): US 200261474 A 20020131
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20030154210 A1 48 G06F-007/00

Abstract (Basic): US 20030154210 A1
NOVELTY - The structure includes a set of sub-networks, each sub-network is stored based on a set of numerical indices that are present in a relational database of the structure. The set of indices for each of the **sub - network** includes a primary index and a set of secondary indices. The indices are derived from a set of **output** functions of the **sub - networks** .
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a sub-network record management system.
USE - Used for storing sub-networks.
ADVANTAGE - The indexing scheme stores and identifies the pre-tabulated sub-networks. The indexing scheme allows efficient identification and storing of the multi-function sub networks.
DESCRIPTION OF DRAWING(S) - The drawing shows the software architecture of a logic synthesizer.
Logic synthesizer (100)
Data generator (115)
Global optimizer (110)
Circuit network design (135)
Power engine (140)
pp; 48 DwgNo 1/26
Title Terms: DATA; STORAGE; STRUCTURE; SET; SUB; NETWORK; STORAGE; BASED; SET; INDEX; DERIVATIVE; OUTPUT; FUNCTION; SUB; NETWORK
Derwent Class: T01
International Patent Class (Main): G06F-007/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-F05E; T01-F05G5; T01-N02A2

7/9/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015649021 **Image available**
WPI Acc No: 2003-711204/200367
XRPX Acc No: N03-568763
Technology mapping performing method for integrated circuit design, involves replacing selected sub - network **with** replacement sub - network **which is identified based on parameter representing** output **function of selected** sub - network
Patent Assignee: HETZEL A (HETZ-I); TEIG S (TEIG-I)
Inventor: **HETZEL A ; TEIG S**
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 20030154449 A1 20030814 US 200261719 A 20020131 200367 B

Priority Applications (No Type Date): US 200261719 A 20020131
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20030154449 A1 48 G06F-017/50

Abstract (Basic): US 20030154449 A1

NOVELTY - A candidate sub-network with graph structure different from tree structure or micro-leaf directed acyclic graph structure is selected from a received design. A parameter is generated based on **output** function of the **sub - network** . A replacement **sub - network** is identified from a storage based on the parameter and replaced with selected sub-network

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for technology mapping performing program.

USE - For performing technology mapping in integrated circuit design.

ADVANTAGE - Allows efficient storing and identification of multi-element and multi-function sub-network.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart explaining the technology mapping performing process.

pp; 48 DwgNo 2/26

Title Terms: TECHNOLOGY; MAP; PERFORMANCE; METHOD; INTEGRATE; CIRCUIT; DESIGN; REPLACE; SELECT; SUB; NETWORK; REPLACE; SUB; NETWORK; IDENTIFY; BASED; PARAMETER; REPRESENT; OUTPUT; FUNCTION; SELECT; SUB; NETWORK

Derwent Class: T01; U11

International Patent Class (Main): G06F-017/50

File Segment: EPI

Manual Codes (EPI/S-X): T01-J15A2; T01-S03; U11-G01

7/9/6 (Item 1 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

01049668 **Image available**

METHOD AND APPARATUS FOR SYNTHESIS

PROCEDE ET DISPOSITIF DE SYNTHESE

Patent Applicant/Assignee:

CADENCE DESIGN SYSTEMS INC, 2655 Seely Avenue, San Jose, CA 95134, US, US (Residence), US (Nationality), (For all designated states except: US)

Patent Applicant/Inventor:

TEIG Steven , 935 College Avenue, Menlo Park, CA 94025, US, US (Residence), US (Nationality), (Designated only for: US)

ASMUS Hetzel, Blankenhainer Strasse 8a, 12249 Berlin, DE, DE (Residence), DE (Nationality), (Designated only for: US

Legal Representative:

ADELI Mani (agent), Stattler Johansen & Adeli LLP, P.O. Box 51860, Palo Alto, CA 94303-0728, US,

Patent and Priority Information (Country, Number, Date):

Patent: WO 200377630 A2-A3 20030925 (WO 0377630)

Application: WO 2003US2984 20030131 (PCT/WO US03002984)

Priority Application: US 200261459 20020131; US 200262014 20020131; US 200262044 20020131; US 200262017 20020131

Designated States:

(Protection type is "patent" unless otherwise stated - for applications prior to 2004)

AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW

(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT SE SI SK TR

(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG

(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Main International Patent Class: G06F-017/50
Publication Language: English
Filing Language: English
Fulltext Word Count: 28366

English Abstract
A method for pre-tabulating sub-networks. This method (1) generates a sub-network that performs a function (605), (2) generates a parameter based on this function (610), and (3) stores the sub-network in a storage structure based on the generated parameters (635).

French Abstract
Dans certains de ses modes de realisation, cette invention concerne un procede de pre-tabulation de sous-reseaux. Ce procede consiste a: (1) creer un sous-reseau auquel est devolue une fonction; (2) generer un parametre selon cette fonction; et (3) stocker le sous-reseau dans une base a structure de stockage en fonction du parametre genere. Dans d'autres modes de realisation, le sous-reseau cree comporte plusieurs elements de circuit. Dans d'autres modes de realisation encore, le sous-reseau genere s'acquitte d'un ensemble d'au moins deux fonctions. Autres modes de realisation : stockage de chacun des sous-reseaux genere sous forme codee. Dans certains cas, l'invention peut concerner la description d'un mode de conception en termes de circuits. Autres modes de realisation encore : le procede (1) consiste a selectionner un sous-reseau dans un modele de conception, (2) identifier une fonction de sortie executee par le sous-reseau, (3) a partir de la fonction de sortie identifiee, reperer un sous-reseau de rechange dans la structure de stockage des sous-reseaux ; et dans certaines conditions, (4) remplacer le sous-reseau candidat selectionne par le sous-reseau de rechange repere. Dans certains modes de realisation, on reporte un modele dans une banque technologique particuliere. Selon certains modes de realisation, on trouve une structure de stockage de donnees dans laquelle est stockee une pluralite de sous-reseaux selon des parametres tires de leurs fonctions de sortie.

Legal Status (Type, Date, Text)
Publication 20030925 A2 Without international search report and to be republished upon receipt of that report.
Examination 20040115 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20040325 Late publication of international search report
Republication 20040325 A3 With international search report.